IN THE CLAIMS

1-16. (Canceled).

17. (Previously presented) A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces and provided with a plurality of resin injection entrances created on said first side surface and a ventilation hole created on said second side surface;

(b) preparing a wiring substrate having a main surface, preparing a first semiconductor chip fixed on said main surface of said wiring substrate and preparing a second semiconductor chip fixed on said first semiconductor chip;

(c) placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c) injecting resin concurrently from the plurality of resin injection entrances toward the second side surface of the cavity in order to seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip, and

wherein in said step (c), said wiring substrate, said first semiconductor chip, and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of said first semiconductor chip is smaller than the length of said second semiconductor chip.

Claim 18 (Canceled).

19. (Original) A semiconductor device manufacturing method according to claim 17, wherein said mold has an air hole created on said second side surface of said cavity.

20. (Previously presented) A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and

fourth side surfaces facing each other and coming in contact with said first and second side surfaces and provided with a plurality of resin injection entrances created on said first side surface and a ventilation hole created on said second side surface;

(b) preparing a wiring substrate having a main surface and a plurality of device areas created thereon, preparing first semiconductor chips fixed on each of said device areas of said wiring substrate and preparing second semiconductor chips fixed on each of said first semiconductor chips;

(c) placing said wiring substrate, said first semiconductor chips and said second semiconductor chips inside said cavity, and then collectively cover said device areas by using said cavity; and

after said step (c), injecting resin concurrently from the plurality of resin injection entrances toward the second side surface of the cavity in order to collectively seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said first semiconductor chips and said second semiconductor chips are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, said length of each of said first semiconductor chips exceeds said length of

corresponding second semiconductor chips stacked on said first semiconductor chips, and

wherein in said step (c), said wiring substrate, said first semiconductor chips, and said second semiconductor chips are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of each of said first semiconductor chips are smaller than the length of corresponding second semiconductor chips stacked on said first semiconductor chips.

21-43. (Canceled).